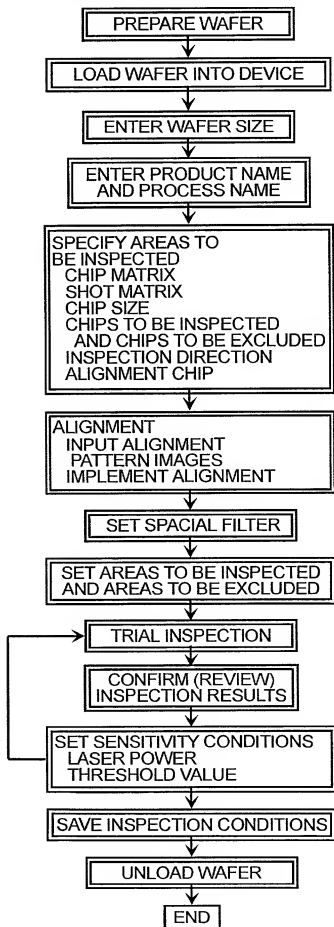


FIG.1

SETTING INSPECTION CONDITIONS (PRIOR ART)

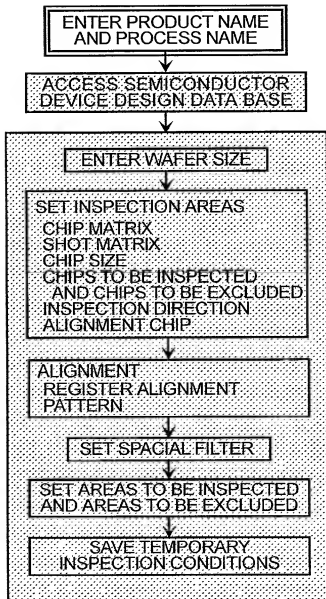


 ITEMS SET AND OPERATED BY WORKER

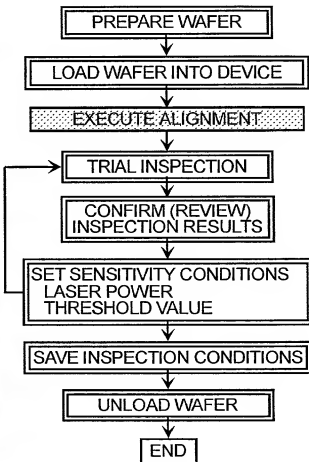
FIG.2

SETTING INSPECTION CONDITIONS

BEFORE WAFER ARRIVES



AFTER WAFER ARRIVES



ITEMS PROCESSED  
AUTOMATICALLY

ITEMS SET AND OPERATED  
BY WORKER

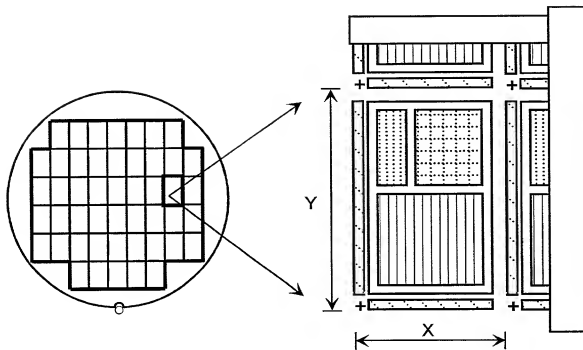
Applicant: Akira Hamamatsu, et al.

Title: Semiconductor Device Inspection Method

Atty Docket No. 16869P-041800

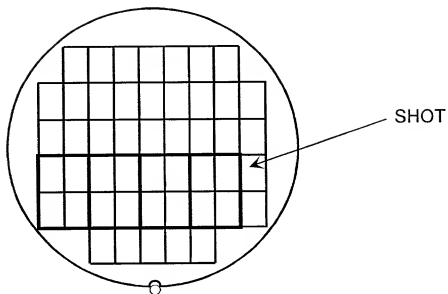
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FIG. 3



SETTING CHIP SIZE

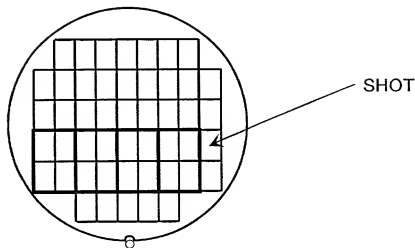
**FIG.4**



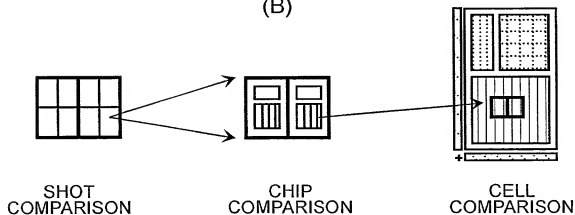
**SETTING SHOT MATRIX**

FIG.5

(A)



(B)



SET THE COMPARISON METHOD TO SUIT THE  
REPETITIVE UNIT

SETTING THE INSPECTION SEQUENCE

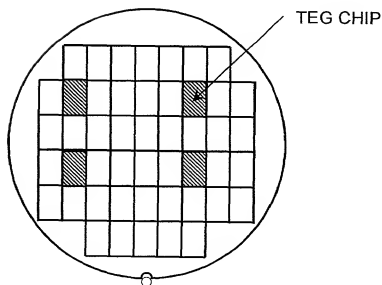
**Applicant:** Akira Hamamatsu, *et al.*

**Title:** Semiconductor Device Inspection Method

**Atty Docket No.** 16869P-041800

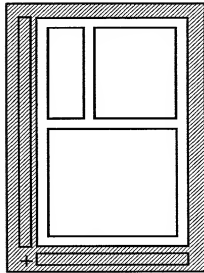
**Sheet 6 of 13**



**FIG.6**



SETTING CHIPS TO BE EXCLUDED  
FROM INSPECTION

**FIG.7**



-  AREAS TO BE INSPECTED
-  AREAS EXCLUDED FROM INSPECTION (SCRIBE AREA)

SETTING AREAS TO BE INSPECTED  
AND AREAS TO BE EXCLUDED

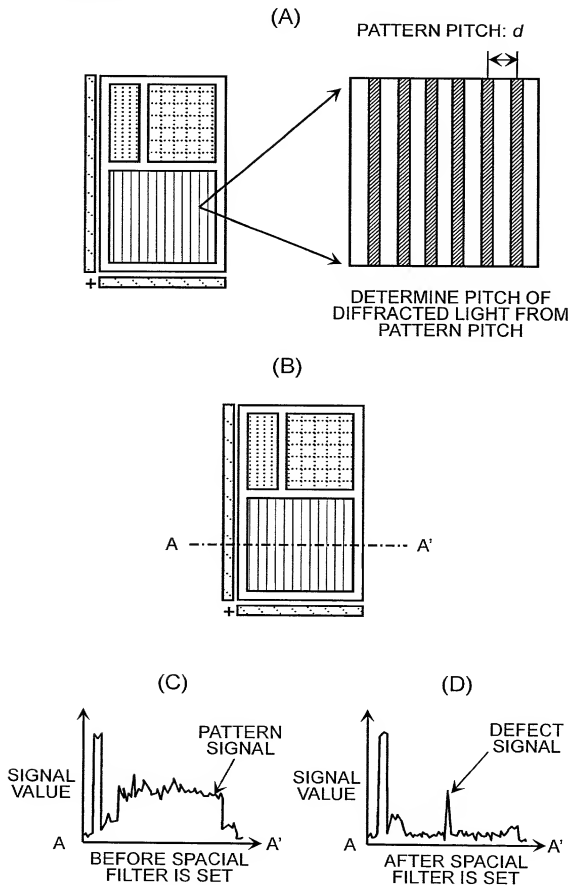
**FIG.8**



SELECT PATTERNS AND MATERIAL  
THAT WILL MAKE IMAGES EASILY  
RECOGNISABLE DURING ALIGNMENT

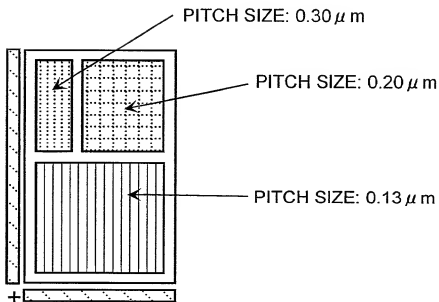
SETTING THE  
ALIGNMENT PATTERN

**FIG. 9**



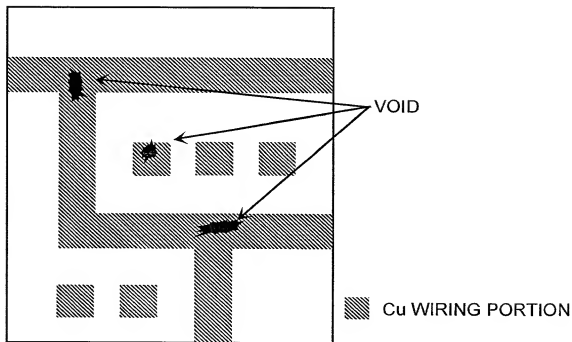


**FIG.10**



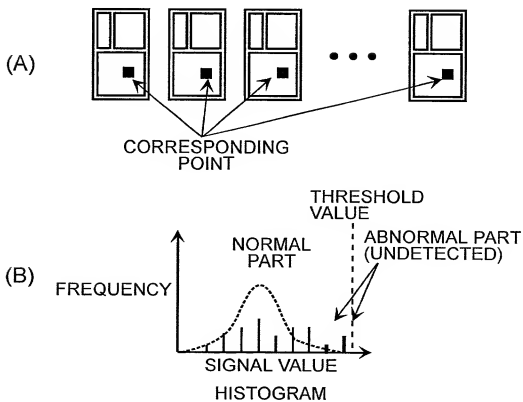
FATALITY JUDGEMENT  
(BY PRODUCT, PROCESS, AND AREA)

FIG.11

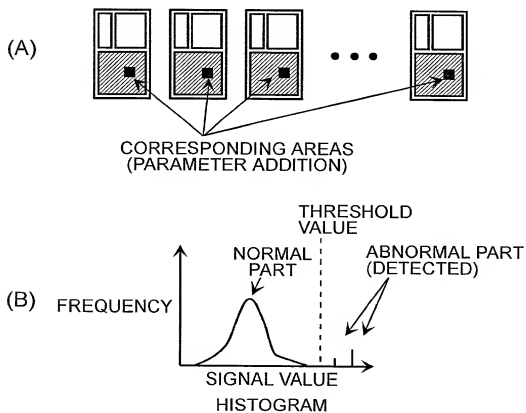


AUTOMATIC DEFECT CLASSIFICATION  
TECHNOLOGY

**FIG.12**



**FIG.13**

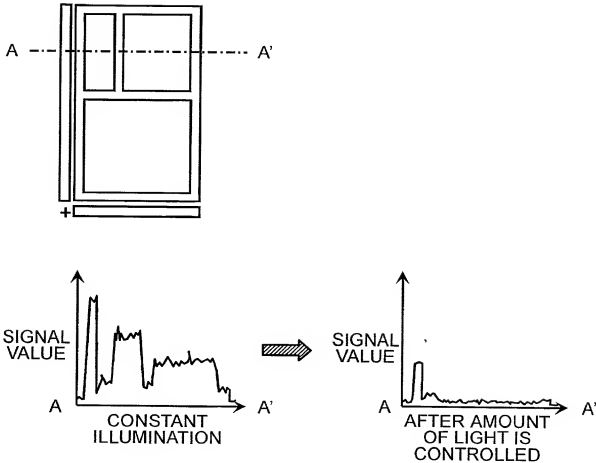


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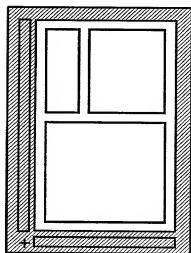
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**FIG.14**

ESTIMATE THE SIGNAL INTENSITY FROM PATTERN  
PITCH AND CONTROL THE AMOUNT OF LIGHT

SETTING THE AMOUNT OF LIGHT

**FIG.15**

AREAS IN WHICH MANY  
FALSE ALARMS OCCUR

( SCRIBE AREA  
AROUND MEMORY MAT )

SETTING AREAS IN WHICH  
MANY FALSE ALARMS OCCUR